

• General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• Features

- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

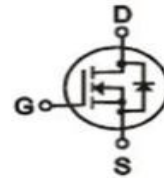
• Application

- BLDC Motor driver
- DC-DC
- Load Switch

• Ordering Information:

Part NO.	ZMS080N08P
Marking	ZMS080N08
Packing Information	TUBE
Basic ordering unit (pcs)	1000

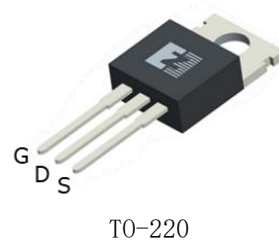
• Product Summary



$$V_{DS} = 80V$$

$$R_{DS(ON)} = 7.5m\Omega$$

$$I_D = 80A$$



• Absolute Maximum Ratings ($T_C=25^\circ C$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		80	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^\circ C$	80	A
	I_D	$T_C=75^\circ C$	65	A
	I_D	$T_C=100^\circ C$	53	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25^\circ C$;	320	A
Total Power Dissipation	P_D	$T_C=25^\circ C$	125	W
Total Power Dissipation	P_D	$T_A=25^\circ C$	2.0	W
Operating Junction Temperature	T_J		-55 to +150	$^\circ C$
Storage Temperature	T_{STG}		-55 to +150	$^\circ C$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1mH$, $V_{GS}=10V$, $R_g=25\Omega$,	50	mJ
		$L=0.5mH$, $V_{GS}=10V$, $R_g=25\Omega$,	105	mJ
ESD Level (HBM)	CLASS 2			

•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	1	°C/W
Thermal resistance, junction-ambient ^①	R_{thJA}		-	62	°C/W
Soldering temperature	T_{sold}		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	80			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.3	1.8	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=80V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=12A$		7.5	9.5	m Ω
		$V_{GS}=4.5V, I_D=8A$		11.0	14	m Ω
Forward Transconductance	g_{FS}	$V_{GS}=5V, I_{SD}=10A$		10		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=12A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	1720	-	pF
Output capacitance	C_{oss}		-	1250	-	
Reverse transfer capacitance	C_{rss}		-	252	-	
Gate Resistance	R_g	$f=1MHz$	-	2		Ω
Total gate charge	Q_g	$V_{DD}=15V, I_D=20A, V_{GS}=10V$	-	23	-	nC
	$Q_g(4.5V)$		-	6.2	-	
Gate - Source charge	Q_{gs}		-	4.6	-	
Gate - Drain charge	Q_{gd}		-	4.4	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	7.3	-	ns
Turn-ON Rise time	t_r		-	13	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	20	-	ns
Turn-Off Fall time	t_f		-	7.5	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, dI_S/dt=100A/\mu s, I_S=20A$	-	39	-	ns
Reverse Recovery Charge	Q_{RR}		-	30	-	nC

Fig.1 Gate-Charge Characteristics

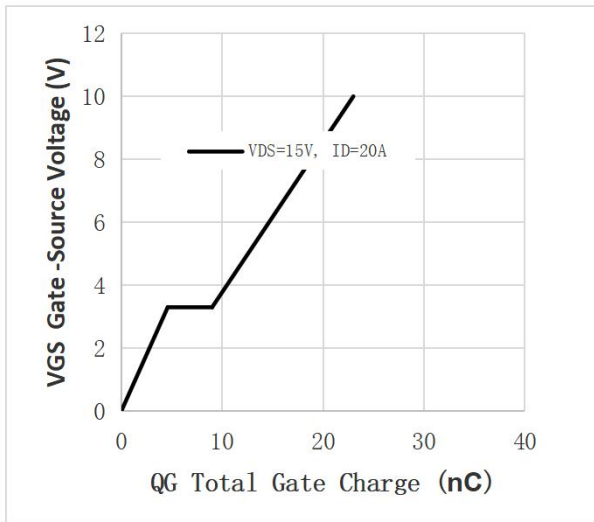


Fig.2 Capacitance Characteristics

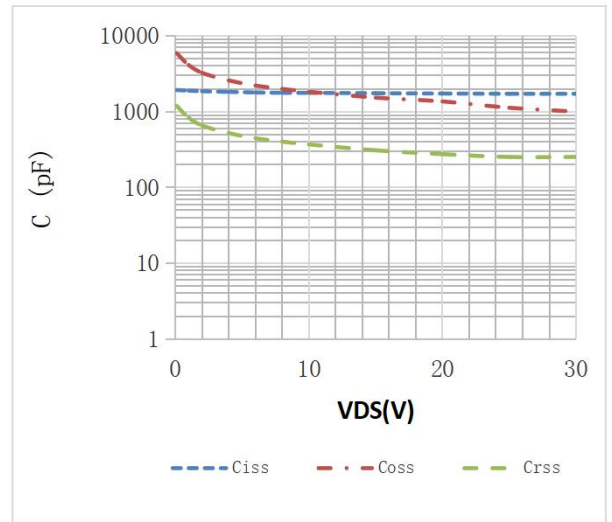


Fig.3 Power Dissipation

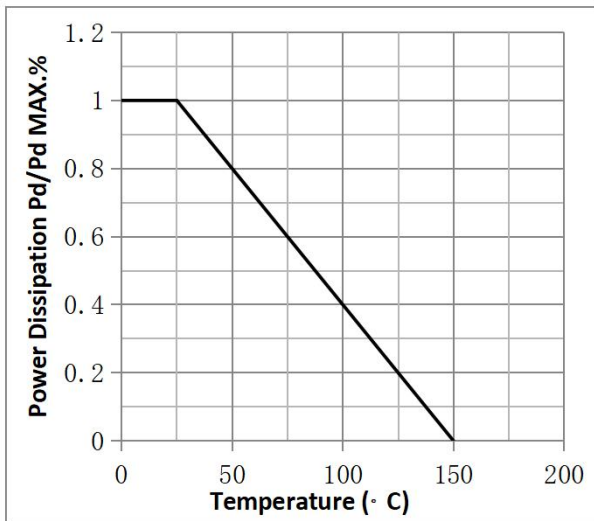


Fig.4 Typical output Characteristics

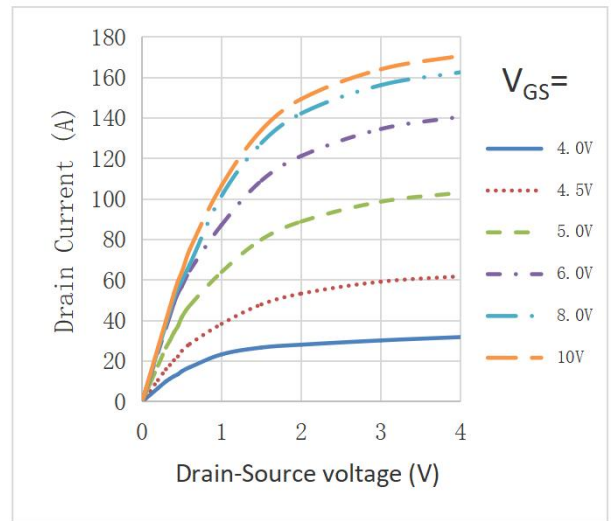


Fig.5 Threshold Voltage V.S Junction Temperature

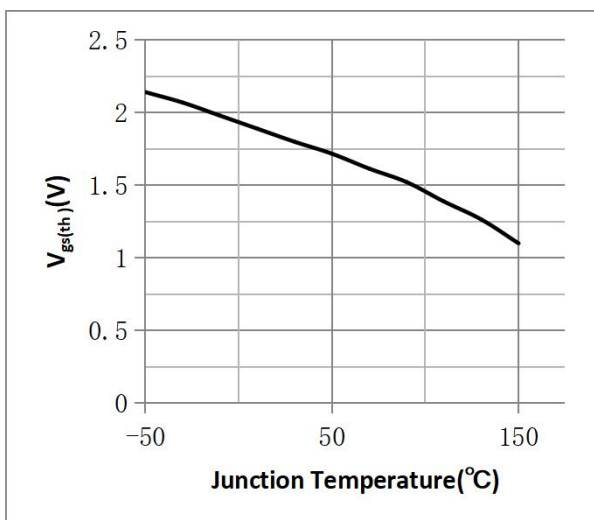


Fig.6 Resistance V.S Drain Current

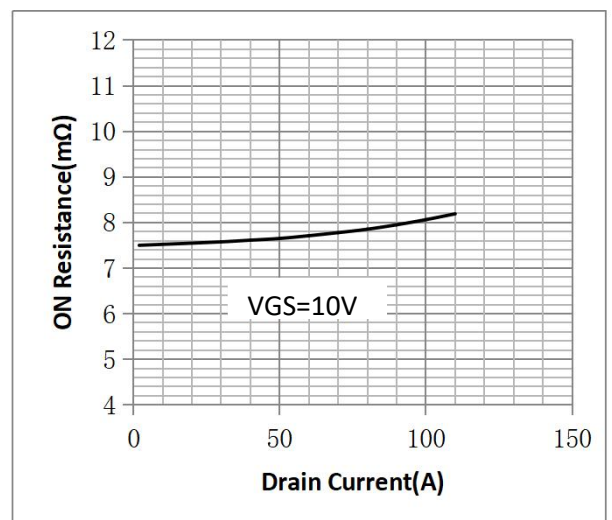


Fig.7 On-Resistance VS Gate Source Voltage

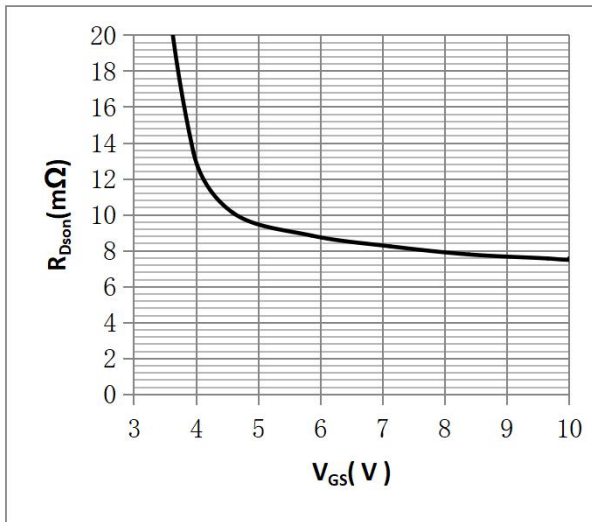


Fig.8 On-Resistance V.S Junction Temperature

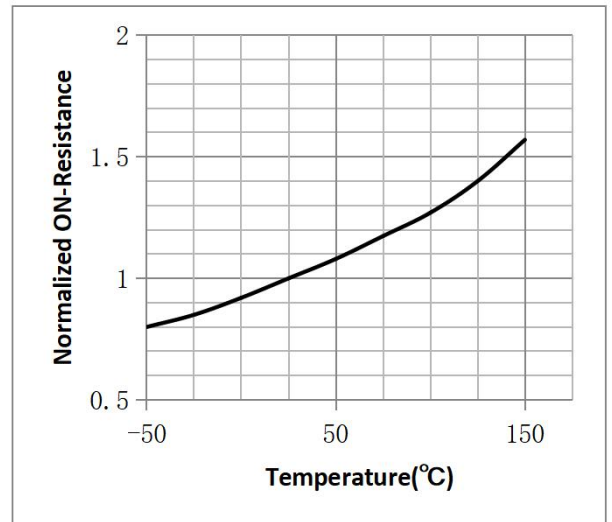


Figure 9. Diode Forward Voltage vs. Current

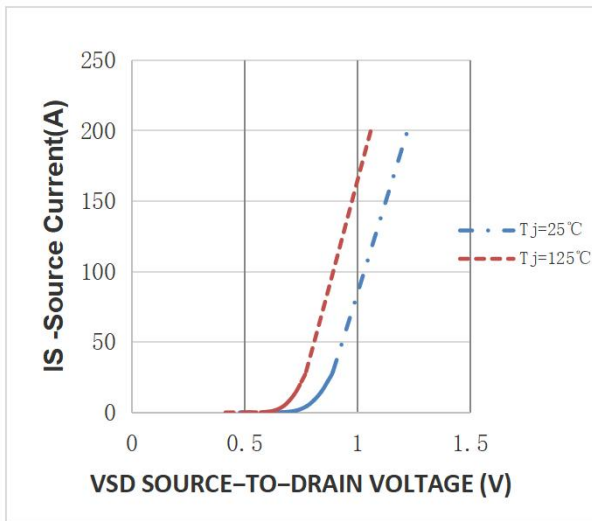


Figure 10. Transfer Characteristics

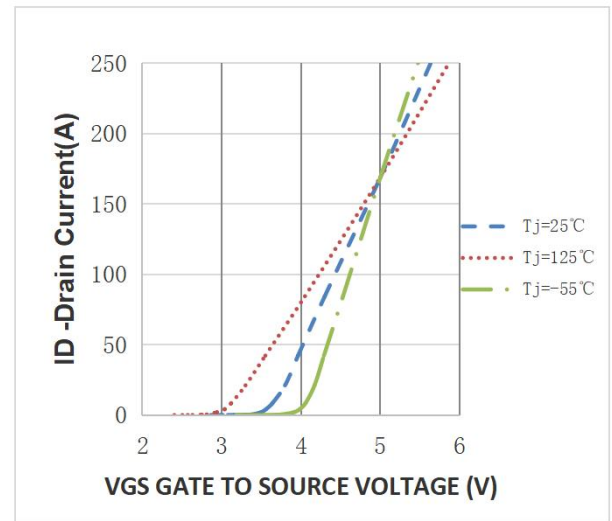


Fig.11 SOA Maximum Safe Operating Area

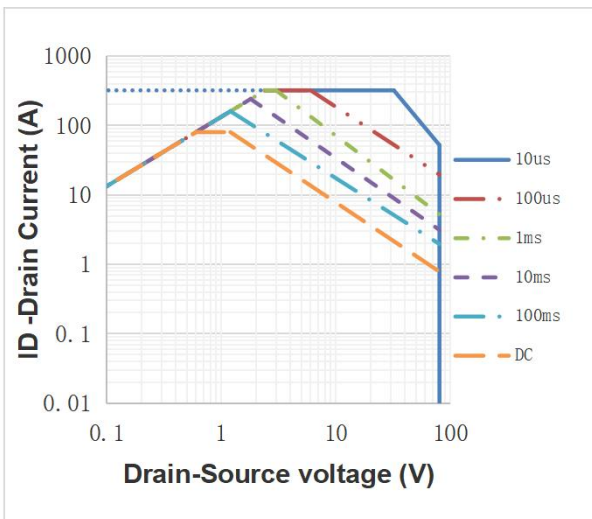
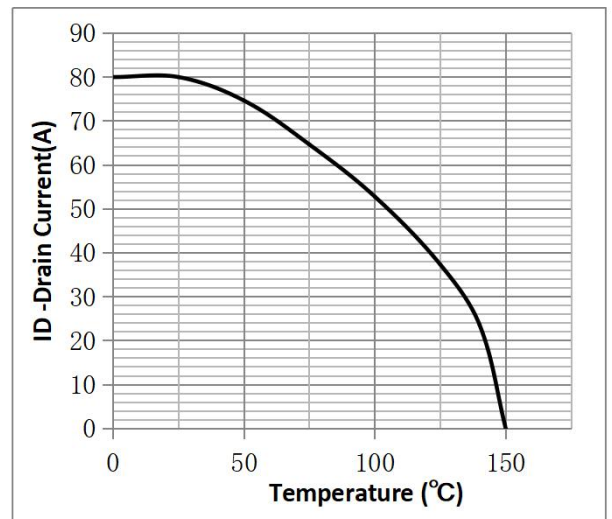
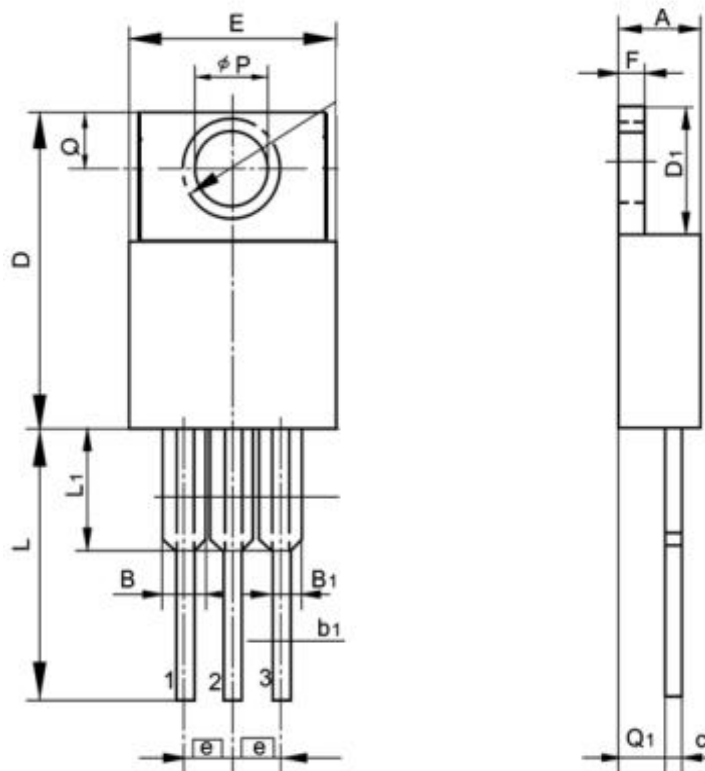


Fig.12 I_D vs. Case Temperature②



•TO-220 Package Outline

SYMBOL	min	nom	max	SYMBOL	min	nom	max
A	4.00		4.80	E	9.90		10.70
B	1.20		1.50	e		2.54	
B1	1.00		1.40	F	1.10		1.45
b1	0.65		1.00	L	12.50		14.50
c	0.35		0.75	L1	3.00	3.50	4.00
D	15.00		16.50	Q	2.50		3.00
D1	5.90		6.90	Q1	2.00		3.00
				ΦP	3.60		3.90



Note:

- ① Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ② Practically the current will be limited by PCB, thermal design and operating temperature.
VGS=10V.

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Revision History

Version	Date	Change
A	2021. 5. 10	
B	2022. 5. 25	Add Rg
C	2022. 10. 22	1. Add Reach, HF figure 2. ID modify
D	2023. 9. 26	1. Modify the package outline diagram